Amendments to the Claims:

This listing will replace all prior versions, and listing, of claims in the application.

1. (currently amended) A method ~~to improve~~ to create a solder bump ~~reliability~~ for interconnection of flip chip devices, comprising the steps of:

providing a substrate, at least one [[a]] contact pad having been provided over ~~the surface of~~ said substrate, a layer of passivation having been deposited over ~~the surface of~~ said substrate, said layer of passivation having been patterned ~~and etched~~, exposing ~~the surface of~~ said at least one contact pad, a layer of ~~Under Ball Metal~~ Under-Bump-Metallurgy (UBM) having been deposited over ~~the surface of~~ said layer of passivation including the exposed ~~surface of~~ said at least one contact pad;

creating at least one T-shaped layer of solder compound over ~~the surface of~~ said layer of UBM in at least one opening created in a layer of patterning material, said at least one T-shaped layer of solder compound being aligned with said at least one contact pad having been provided over ~~the surface of~~ said substrate, said creating at least one T-shaped layer of solder compound over said layer of UBM comprising:

(i) depositing said layer of patterning material over said layer of UBM; and

(ii) patterning and developing said layer of patterning material using a grey-tone mask;

removing said layer of patterning material, leaving in place said at least one T-shaped layer of solder compound, exposing ~~the surface of~~ said ~~patterned layers~~ layer of UBM;

etching said exposed layer of UBM using said at least one T-shaped layer of solder compound as a mask; and

reflowing ~~the surface of~~ said solder compound, creating said solder bump.

2. (original) The method of claim 1, said layer of patterning material comprising photoresist.

3. (original) The method of claim 1, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

4. (original) The method of claim 1, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

5. (currently amended) The method of claim 1, said passivation layer deposited over ~~the surface of~~ said semiconductor surface comprising a plurality of passivation layers.

6. (original) The method of claim 5, at least one of said plurality of passivation layers being selected from the group consisting of PE Si_3N_4 and SiO_2 and a photosensitive polyimide and phosphorous doped silicon dioxide and titanium nitride.

7. (currently amended) The method of claim 1, said at least one contact pad on said semiconductor ~~surface~~ substrate being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

8. (currently amended) The method of claim 1, said at least one contact pad on said semiconductor substrate further being expanded to include a contact pad that is formed on a surface that is selected from the group of surfaces consisting of printed circuit boards and flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

9. (currently amended) The method of claim 1 with an additional step of applying a solder flux to ~~the surface of~~ said solder compound, said additional step ~~to be~~ being performed immediately prior to said reflowing ~~the surface of~~ said solder compound.

10. (currently amended) The method of claim 1, said step of patterning and etching said layer of UBM being further expanded, leaving said layer of UBM in place above and extending from above said at least one contact pad ~~by a measurable amount~~, simultaneously creating conductive interconnect lines on ~~the surface of~~ said layer of passivation, said conductive interconnect lines making contact with at least one contact pad on said semiconductor substrate by creating openings in said layer of passivation that align with at least one contact pad on said semiconductor substrate.

Claim 11. (cancelled).

12. (currently amended) The method of claim [[11]] 1 wherein said grey-tone mask comprises:

at least one pattern of two concentric patterns of opaque material, said at least one pattern of two concentric patterns comprising a first pattern and a second pattern;

[[a]] said first pattern of said two concentric patterns of opaque material being a pattern that surrounds said second pattern, said first pattern having a first thickness;

[[a]] said second pattern of said two concentric patterns surrounding a transparent surface area of said grey-tone mask, said transparent surface area being aligned with said at least one contact pad provided on ~~the surface of~~ said substrate, said second pattern having a second thickness; and

said first thickness being larger than said second thickness ~~first pattern having a thickness that is larger than a thickness of said first pattern by a measurable amount~~.

13. (currently amended) The method of claim [[11]] 1, with an additional step of performing an in-situ sputter clean of inside surfaces of said at least one opening having a T-shape created through said layer of patterning material ~~and said exposed surface of said layer of UBM~~.

14. (currently amended) The method of claim 13, with an additional step of depositing a seed layer over inside surfaces of said at least one opening having a T-shape created through said layer of patterning material ~~and said exposed surface of said layer of UBM~~.

15. (currently amended) A method ~~to improve~~ to create a solder bump ~~reliability~~ for interconnection of flip chip devices, comprising the steps of:

providing a substrate, active semiconductor devices having been created in or on ~~the surface of~~ said substrate;

creating at least one [[a]] contact pad over ~~the surface of~~ said substrate;

depositing a layer of passivation ~~having~~ over ~~the surface of~~ said substrate, including ~~the surface of~~ said at least one contact pad;

patterning ~~and etching~~ said layer of passivation, exposing ~~the surface of~~ said at least one contact pad;

depositing a layer of ~~Under Ball Metal~~ Under-Bump-Metallurgy (UBM) over ~~the surface of~~ said layer of passivation, including ~~the exposed surface of~~ said at least one contact pad;

depositing a layer of exposure sensitive material over ~~the surface of~~ said layer of UBM;

patterning ~~and etching~~ said layer of exposure sensitive material, creating at least one opening having a T-shaped cross section through said exposure sensitive material, said at least one opening being aligned with said at least one contact pad created over ~~the surface of~~ said substrate, said creating at

least one opening having a T-shaped cross section through said exposure sensitive material comprising:

(i) depositing said layer of exposure sensitive material over said layer of UBM; and

(ii) patterning and developing said layer of exposure sensitive material using a grey-tone mask;

filling said at least one opening created through said exposure sensitive material with a solder compound;

removing said exposure sensitive material from ~~the surface of~~ said layer of UBM, leaving in place at least one T-shaped layer of solder compound, exposing ~~the surface of~~ said layer of UBM;

etching said layer of UBM, using said at least one T-shaped layer of solder compound as a mask; and

reflowing said at least one T-shaped layer of solder compound.

16. (original) The method of claim 15, said layer of exposure sensitive material comprising photoresist.

17. (original) The method of claim 15, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

18. (original) The method of claim 15, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

19. (currently amended) The method of claim 15, said passivation layer deposited over ~~the surface of~~ said semiconductor surface comprising a plurality of passivation layers.

20. (original) The method of claim 19, at least one of said plurality of passivation layers being selected from the group consisting of PE Si_3N_4 and SiO_2 and a photosensitive polyimide and phosphorous doped silicon dioxide and titanium nitride.

21. (currently amended) The method of claim 15, said at least one contact pad on said semiconductor surface being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

22. (currently amended) The method of claim 15, said at least one contact pad on said semiconductor substrate further being expanded to include a at least one contact pad that is formed on

a surface that is selected from the group of surfaces consisting of printed circuit boards and flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

23. (currently amended) The method of claim 15, with an additional step of applying a solder flux to ~~the surface of~~ said solder compound, said additional step ~~to be~~ being performed immediately prior to said reflowing ~~the surface of~~ said solder compound.

24. (currently amended) The method of claim 15, said step of patterning and etching said layer of UBM being further expanded, leaving said layer of UBM in place above and extending from above said at least one contact pad by a measurable amount, simultaneously creating conductive interconnect lines on ~~the surface of~~ said layer of passivation, said conductive interconnect lines making contact with at least one contact pad on said semiconductor substrate by creating openings in said layer of passivation that align with at least one contact pad on said semiconductor substrate.

Claim 25: (cancelled).

26. (currently amended) The method of claim [[25]] 15 wherein said grey-tone mask comprises:

at least one pattern of two concentric patterns of opaque material, said at least one pattern of two concentric patterns comprising a first pattern and a second pattern;

[[a]] said first pattern of said two concentric patterns of opaque material being a pattern that surrounds said second pattern, said first pattern having a first thickness;

[[a]] said second pattern of said two concentric patterns surrounding a transparent surface area of said grey-tone mask, said transparent surface area being aligned with said at least one contact pad provided on ~~the surface of~~ said substrate, said second pattern having a second thickness; and

said first thickness being larger than said second thickness ~~first pattern having a thickness that is larger than a thickness of said first pattern by a measurable amount~~.

27. (currently amended) The method of claim [[25]] 15, with an additional step of performing an in-situ sputter clean of inside surfaces of said at least one opening having a T-shape created through said layer of patterning material ~~and said exposed surface of said layer of UBM~~.

28. (currently amended) The method of claim 27, with an additional step of depositing a seed layer over inside surfaces of said at least one opening having a T-shape created through said layer of patterning material ~~and said exposed surface of said layer of UBM~~.

Please add the following new claims:

29. A solder bump for interconnection of flip chip devices, comprising:

a substrate, active semiconductor devices having been created in or over said substrate;

at least one contact pad created over said substrate;

a patterned layer of passivation created over said substrate, said patterned layer of passivation exposing said at least one contact pad;

a patterned layer of Under-Bump-Metallurgy (UBM) created over said layer of passivation, including said at least one contact pad, a surface area of the patterned layer of UBM being limited to a size no larger than a size of a surface area of the at least one contact pad; and

at least one layer of reflown solder compound overlying said patterned layer of UBM.

30. The solder bump of claim 29, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

31. The solder bump of claim 29, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

32. The solder bump of claim 29, said patterned layer of passivation comprising a plurality of passivation layers.

33. The solder bump of claim 32, wherein at least one of said plurality of passivation layers is PE Si_3N_4, SiO_2, a photosensitive polyimide, phosphorous doped silicon dioxide or titanium nitride.

34. The solder bump of claim 29, said at least one contact pad on said semiconductor surface being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

35. The solder bump of claim 29, said at least one contact pad on said semiconductor substrate further comprising a contact pad formed on a surface that is selected from the group of surfaces consisting of printed circuit boards and flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

36. The solder bump of claim 29, with a seed layer having been deposited over said patterned layer of passivation.